Release History

Rev	Description	Date	Author
A	Pre-release	3/30/2001	Mike Timmons

006-00021
Tunable Filter Card (TFC)
Module Definition

Approvals	Date
Design Engineer: Mike Timmons	
Engineering Manager:	
Product Management:	
Optical Engineering:	
Systems Engineering:	
Mechanical Engineering:	
Manufacturing:	
QA:	

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5. Introduction

Cinta needs a tunable bandpass filter to lower the ASE noise output from TAD cards. The tunable filter must lock to an unspecified carrier frequency, and track the channel indefinitely, through power fluctuations and frequency perturbations. Tunable filter optics, electronics and firmware are common to both OC48 and OC192 channels.

When the host needs to provision a new laser frequency it tunes the laser accordingly and commands the tunable filter to "Lock-to-Laser" again. Figure 1 illustrates how a TFC fits in a TAD system.

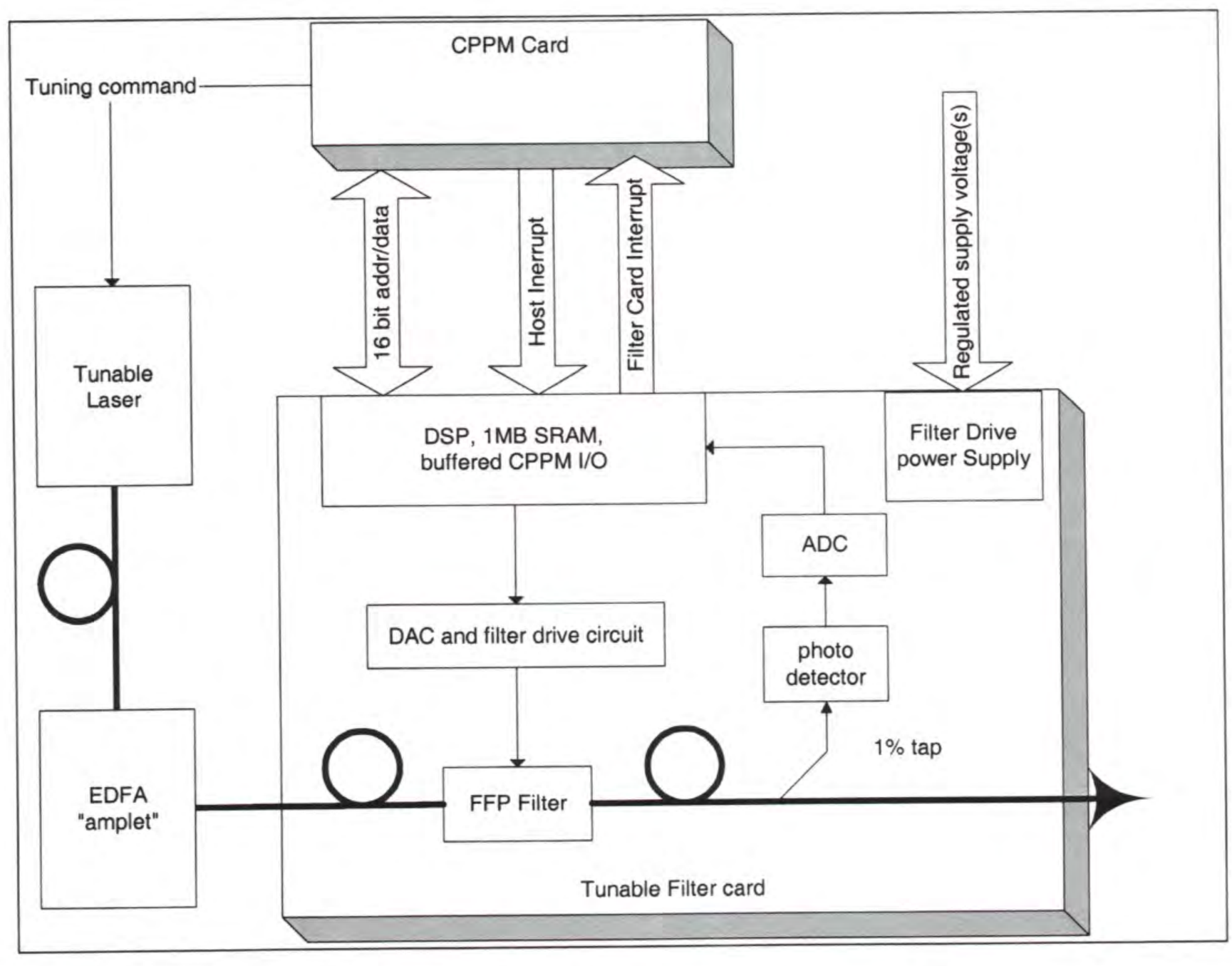


Figure 1: TAD installation of Tunable Filter Card(TFC)

6. Tunable Filter operation

6.1 Filter operation

The tunable fiber Fabry-Perot filter has a free spectral range (FSR) of about 10000 GHz. Basically, it passes output power for the same input frequency every FSR. Figure 2 is a simulated plot to show what this looks like if you sweep 4 resonance orders. In reality, optical transmission is not uniform. It attenuates an additional 0.25dB per FSR, approximately. Nominal filter attenuation is around 2dB.

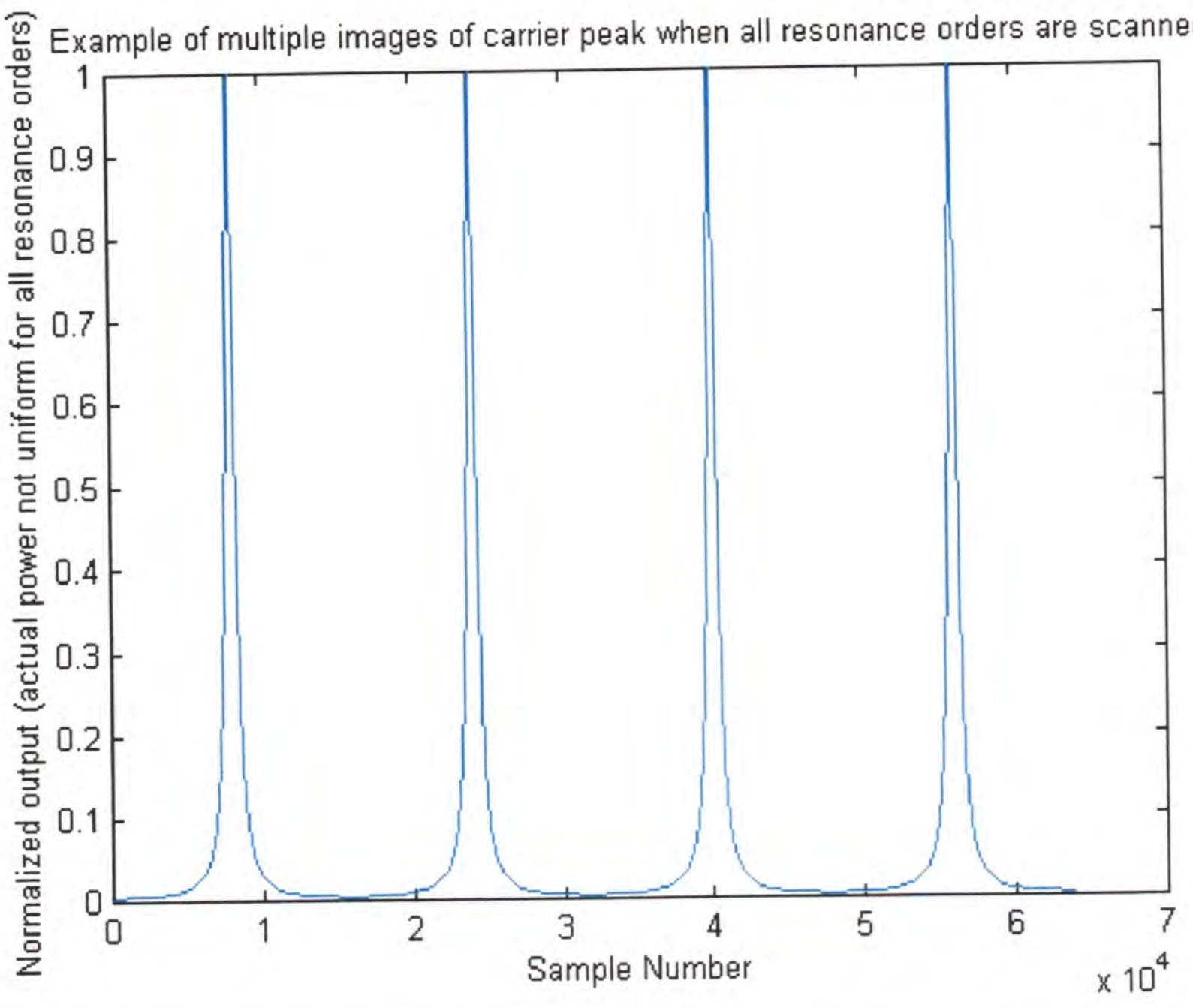


Figure 2: Example of multiple images when scanning multiple FSRs

6.2 Filter Card Operation

6.2.1 TFC state diagram

1. Start in **TFC_FIND** state when commanded by host or when lose lock.
2. **TFC_ACQUIRE** after sample is below noise floor.
3. **TFC_BACKUP** after acquire detects valid channel power.
4. **TFC_PULL_IN** after backup has produced valid pull-in power.
5. **TFC_CHECK** after specified milliseconds of pull-in.
6. **TFC_HOLD** thereafter
7. **TFC_PARKED** to kill tracking loop and hold DAC output at 0 volts. **This is not a "mute" feature. Zero volts of filter drive could place the filter at any wavelength, depending on the filter and the temperature.**

Any of the above steps can encounter an error condition that prompts the TFC to send an error message to the host, and to place itself in **TFC_PARKED** state. Figure 3 illustrates how the TFC moves through the above states during the lock-to-laser process.

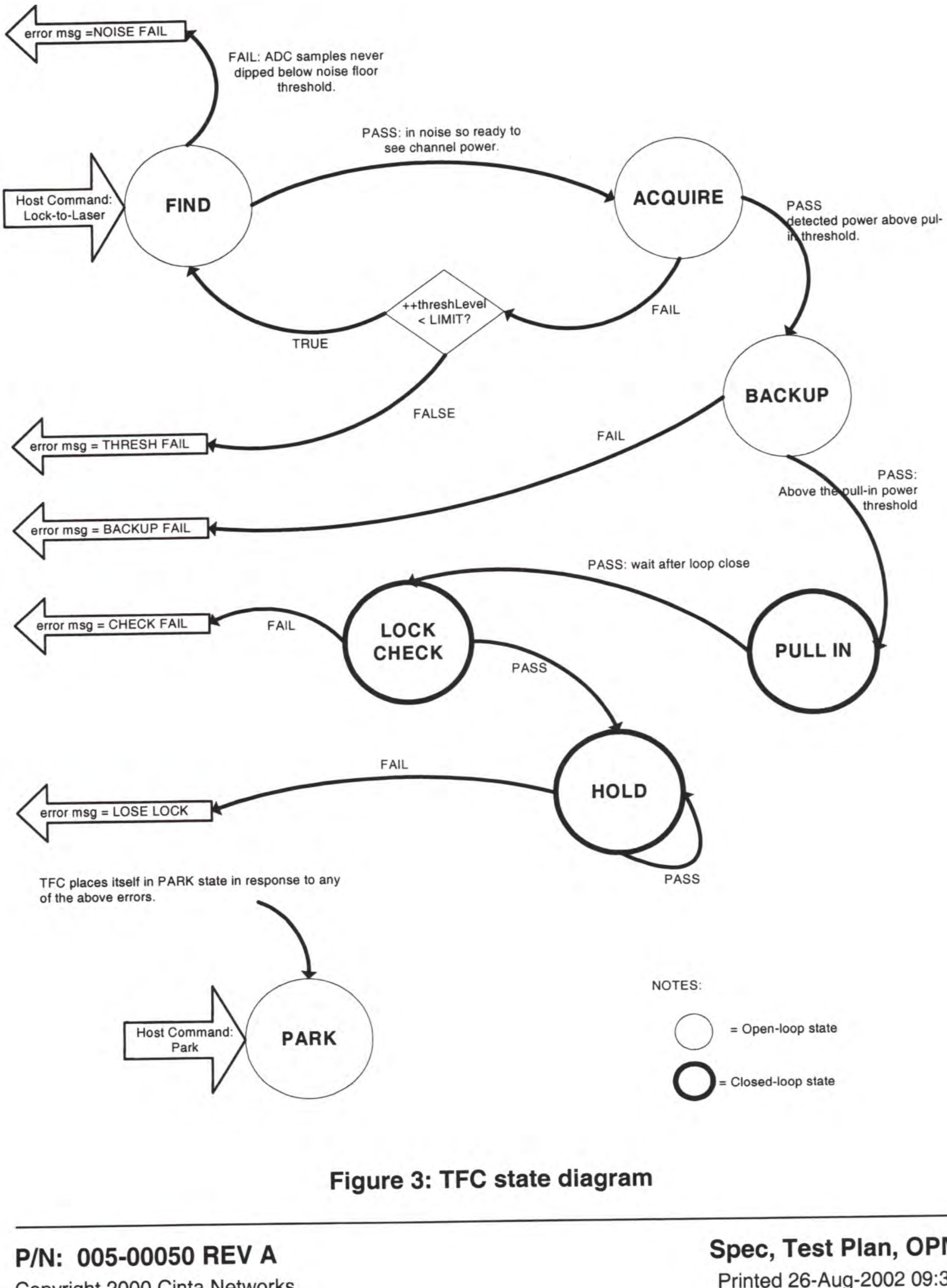


Figure 3: TFC state diagram

6.2.2 TFC state details

The TFC does not know the wavelength of the channel it must track. Every attempt to lock to an optical signal requires a band sweep to detect the channel, and a tracking loop to remain locked to the channel after it is detected. The band sweep is an open-loop technique. The tracking relies on a linear, closed-loop controller. Both the open- and closed-loop modes are under DSP control.

6.2.2.1 Open-loop states

A major lock-time limiter is the acquisition phase: positioning the filter close to the channel to allow the linear control loop to "pull" the filter to the channel when the loop is closed.

In principal, we need to ramp the filter until we see power before closing the loop. Initial experiments indicated that the slope of the initial ramp must be low enough to not overshoot the channel upon loop closure. The following open-loop drive scheme eliminates the overshoot problem, while not consuming as much time as a slow initial ramp.

6.2.2.1.1 TFC_FIND: detect the noise floor

Zero volts of filter drive could place the filter center at any wavelength. When the open-loop ramp commences, we don't want to close the loop on valid power detected immediately. This power could be on the trailing edge of the channel, requiring the loop to drive the filter back to center it on the channel. We might not have enough drive near zero volts, so we force the TFC to "see" the noise floor before preparing for channel lock. Figure 4 shows a peak near the start of a simulated full sweep (4 FSRs) of the filter. We don't want to catch the first peak because the DAC can't drive below zero volts, and that peak is too close.

Instead, If channel power is detected early in the TFC_FIND process, before the noise floor is detected, the TFC will catch the channel in the next free spectral range (FSR) of the filter. Basically, the filter sweeps the same optical band every FSR, so we'll see another image of the channel after we sweep 1 FSR. Looking at Figure 4, the TFC will pick up the second peak from the left. The DAC should have plenty of range to track that one.

Design Idea 1: If the Filter drifts more than 1 FSR due to temperature or aging, it is conceivable that the TFC could lose the channel. Verify filter drift characteristics with Micron Optics.

Considering Design Idea 1, we might rather lock to the third peak in Figure 4. However, if the filter can drift more than 1 FSR we could run out of room on the high side of DAC drive. Verify vendor's filter drift specifications.

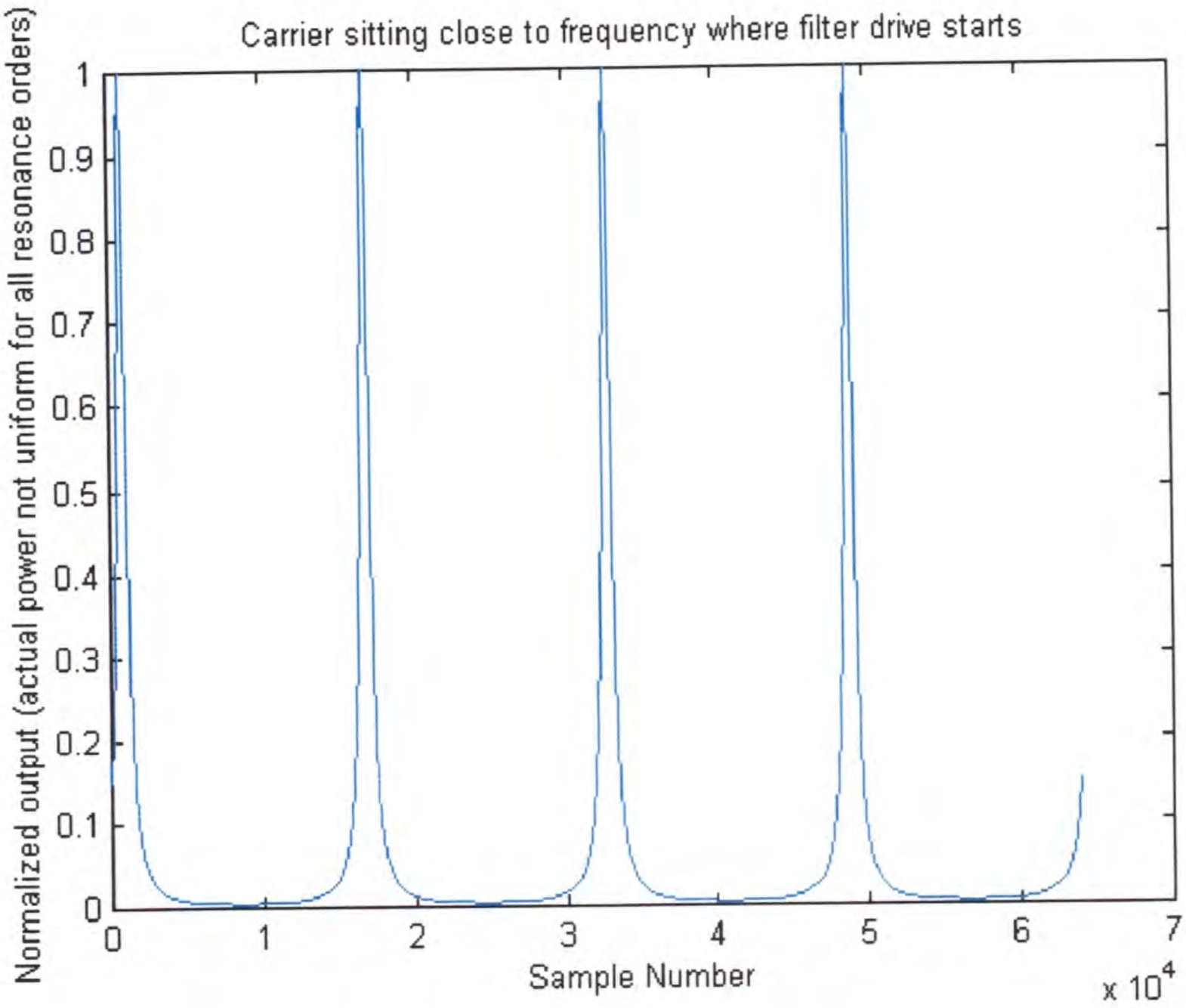


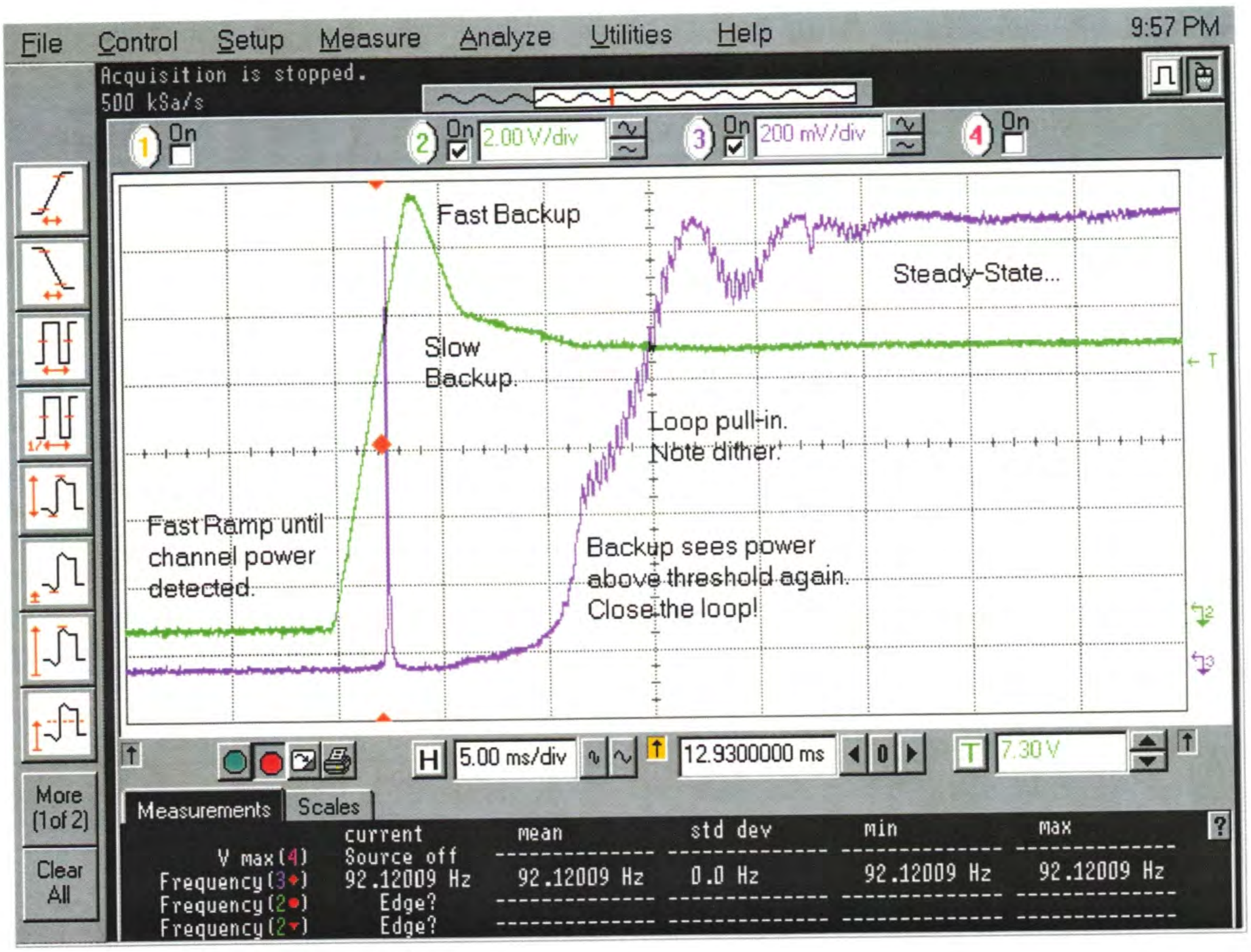
Figure 4: Filter drive start close to carrier frequency.

The filter slew rate in the FIND state is roughly 3ms per FSR. Our total acquire-and-lock goal is 15-30 ms, so the position of the channel relative to the position of the filter at the beginning of the TFC_FIND ramp has little impact on the total lock time. The locking time variance due to channel wavelength is a few milliseconds at most.

6.2.2.1.2 TFC_ACQUIRE

When the TFC sees samples below its noise floor threshold it is ready to assume that future samples above its lock threshold represent the channel to track. The TFC_ACQUIRE mode drives the filter with the same fast ramp that the FIND mode uses, but it is ready to change modes when it sees channel power above its lock

threshold. When it sees this power it knows that the fast ramp has overshot the target, so it reverses the filter drive to "back-up" to the channel.



6.2.2.1.3 TFC_BACKUP

When the TFC sees channel power above its lock threshold during the TFC_ACQUIRE ramp, it switches to a BACKUP state because it knows the fast ramp overshot the channel. The current filter drive is well ahead of our sampler that indicated we have valid channel power (see ADC group delay section below).

The BACKUP mode eats-up a bunch of this overshoot with a quick ramp in the other direction before transitioning to a slower slew rate that will permit a transition from open- to closed-loop once the TFC backs into the filter it passed with the fast ramp.

The transition form the fast backup to the slow backup occurs after some number of samples that resulted from initial experiments. Table 2 indicates current default values for the initial backup slope, final backup slope, and the number of backup samples before backup slope transition.

When the BACKUP state produces valid lock power the TFC closes the linear loop.

6.2.2.2 Closed-loop states

6.2.2.2.1 Closed-loop controller design

Figure 5 shows the control loop governing TFC filter pull-in and channel tracking. The DSP implements drive dither and mixing of samples for phase-sensitive detection of the dither in the samples. The low-pass filter of the mixing product produces an error signal. The loop is linear when the filter is roughly centered on the channel.

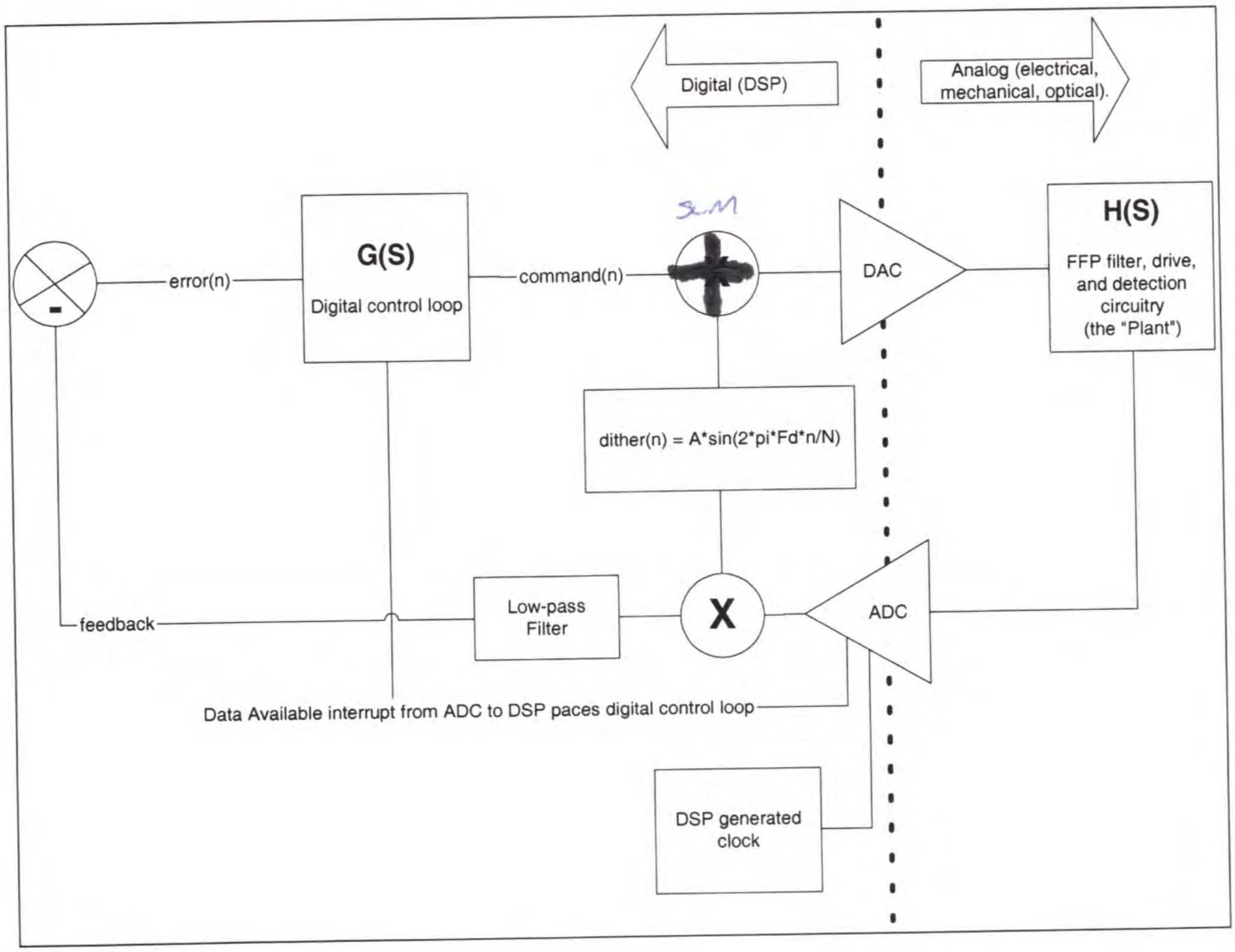


Figure 5: Linear tracking loop

Pull-in is achievable before the loop is in the linear region. The low-pass filter of the mixing product begins producing an error signal of appropriate sign, so the loop will pull-in. However, the error follows a non-linear path as the filter is centered on the channel.

6.2.2.2.1.1.1 System dynamics

6.2.2.2.1.1.1.1 Fabry-Perot Filter

We don't have a precise model for the filter, but we estimate it to be an overdamped second-order system with poles near 1kHz.

6.2.2.2.1.1.2 High-voltage driver

Ideally, the frequency response of the high-voltage drive (HVD) circuit should be well above the mechanical frequency response to effectively remove it from consideration when desining a controller given the open-loop frequency response of the plant.

The current HVD circuit bandwidth is about 1KHz, or in the neighborhood of the mechanical bandwidth. Figure 6 is a copy of a plot on page 127 of data book titled "Steve Yang #1".

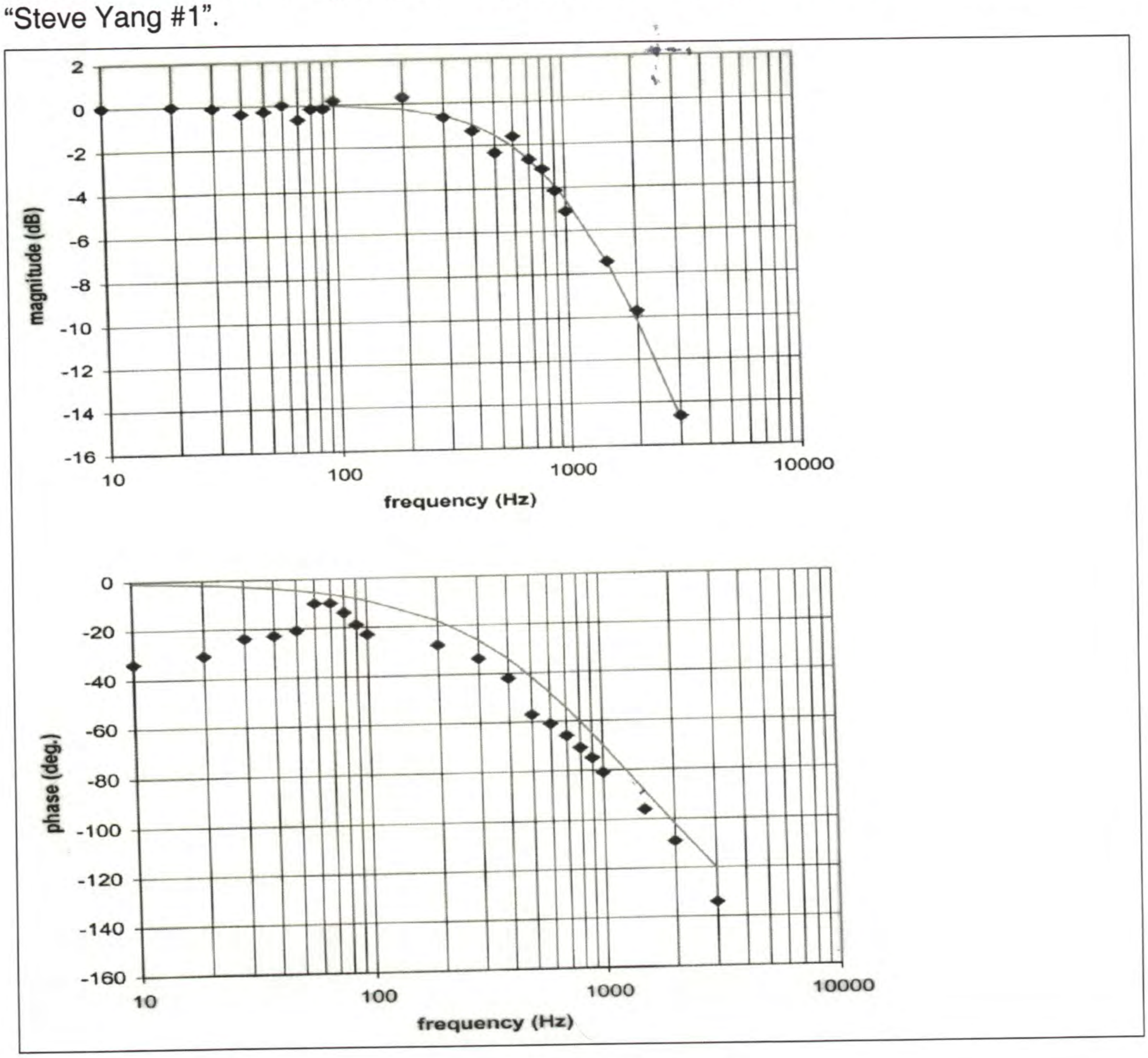


Figure 6: High-Voltage Driver Frequency Response Plot

Speeding-up the HVD might make future tweaking easier, as it will decouple HVD dynamics from the problem. At present, we don't know the relative impact of the HVD bandwidth and the mechanical bandwidth on the loop bandwidth of our system.

- "Steven T. Yang lab book #2" contains equations for HVD frequency response on page 53. Surrounding pages address HVD design using the Apex Op-Amp we are using.

Design Idea 2: Speed-up HVD, but ADC group delay is major limiter, so try 1x decimation for the ADC first (see section 6.2.2.2.1.1.1.4).

6.2.2.2.1.1.1.3 Photodetector and TIA circuit.

"Steven T. Yang lab book #2" addresses TIA design on pages 14-26. In adjusting the gain of the TIA for the TFC the TIA bandwidth was not computed. The gain is lower than the gain used in the same circuit on the OPM, and no distortion of an input signal during a sweep was evident in early TFC experiments. TIA bandwidth hasn't appeared as a potential performance issue so it is assumed to be substantially greater than the bandwidth of other loop elements.

6.2.2.2.1.1.1.4 ADC group delay

We use an over-sampling and decimating ADC: the Analog Devices AD9260. It introduces a group delay to our system that produces the dominant poles in our loop.

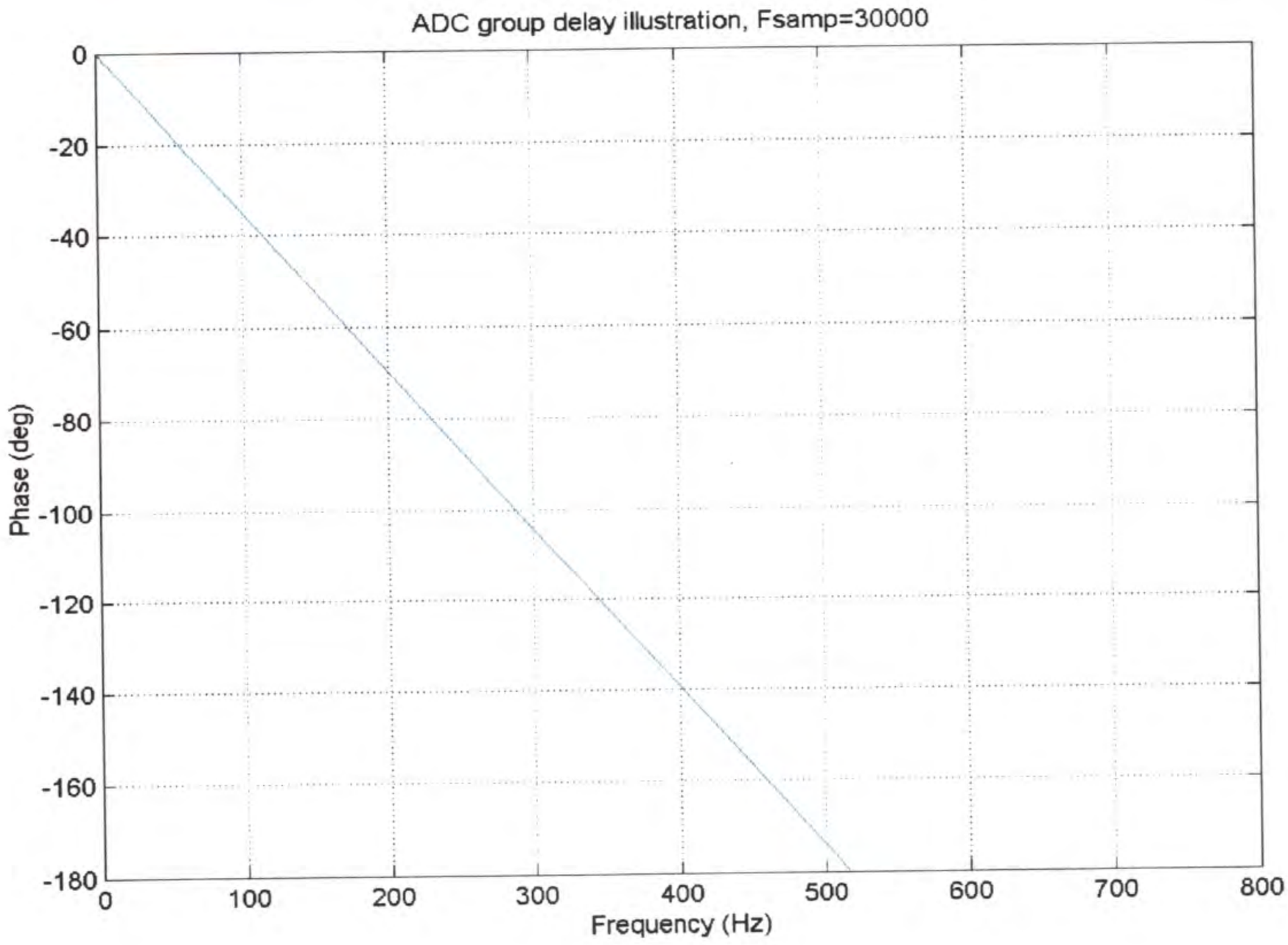


Figure 7: ADC group delay illustration

If you assume the HVD and Fabry-Perot poles are above 1KHz, the phase delay they introduce doesn't come into effect until long after the ADC group delay has destroyed loop bandwidth.

Fortunately, our controller has been tuned to work under this group delay, and the loop seems plenty fast for tracking slight variations in channel frequency. However, the open-loop acquisition scheme is sensitive to the group delay. In fact, hindsight indicates that the group delay motivated the "ramp-and-backup" scheme.

Figure 8 illustrates the ramp-and-backup scheme. When the TFC detects the pink peak in the figure it starts to "backup" the filter. The yellow trace in the figure is the filter drive signal. Notice the roughly 1ms delay between the actual time the filter passes the peak and the time the TFC starts to backup. Most, if not all, of this delay can be attributed to the ADC group delay.

Figure 8: ADC group delay impact on open-loop performance.

Page 5 of the Analog Devices AD9260 (Cinta PN 140-00033) data sheet indicates the absolute group delay for 8-times decimation to be…

- Tdelay = 13.55 x (20MHz / Fclk) microseconds
  - Say Fclk = 8 x Fsamp = 8 x 30KHz = 240 KHz…
  - Tdelay = 1.1 ms

Design Idea 3: Eliminate excessive ADC group delay by trying ADC in 1x decimation mode. Mike Timmons briefly tried using the ADC in "1x Mode", but the samples exhibited a severe offset. The data sheet indicates a different output scaling for 1x mode, but that didn't seem to explain the problem Mike was having. Trying the ADC in 1x mode is the FIRST THING TO TRY if you want the speed-up the loop. You'll be forced to live with less ADC resolution, but we don't need much in this application.

6.2.2.2.1.1.2 Controller design

The Tunable filter and high-voltage driver are overdamped (low Q), so we don't need to design around any resonance issues. We also don't have a good model of the plant[1]. Without a good model it is tough to cook-up a good theoretical compensator design (lead-lag for example). Instead, the compensator is in the form of a PID (proportional, integral, derivative) controller that is easy to tune. Mike, add link to PID notes.

This is how Mike Timmons arrived at the initial design…

- Organize the compensator parameters into classic PID form.
- Zero integral and derivative terms.
- Tweak proportional gain until loop pulls-in, locks, and remains stable.
- Follow tuning rules to investigate impact of integral and derivative terms

6.2.2.2.2 TFC_PULL_IN

For the loop to lock quickly we want to close the loop when the filter is near the channel center frequency. This results in the fastest pull-in time.

During pull-in the TFC applies a dither signal whose amplitude decreases over time. See dither parameters described in Table 2. This decreasing dither amplitude is basically a dynamically scaled gain: the larger dither amplitude produces a larger error signal output from the phase-sensitive detector, so we get bigger gain during pull-in. The stead-state dither amplitude is chosen so as not to produce visible ripple in the filter output. The dither amplitudes are specified in terms of DAC counts.

6.2.2.2.3 TFC_CHECK

After the pull-in time expires the TFC should be locked to the center of the channel. A FIFO of about 50 samples is maintained for looking at the input signal sample average over a brief period in time. At present, if the FIFO sample mean is above the noise floor we indicate valid lock.

Design Idea 4: Modify Lock check to make it less forgiving if you require a better measurement of filter transmission before indicating a valid lock.

6.2.2.2.4 TFC_HOLD

[1] Mike Timmons also didn't calculate the ADC pipeline delay correctly, so the original plant model was way off.

In hold mode the TFC keep the same FIFO running that was used for the lock check. The TFC will send an error message to the host if the sample mean of the FIFO falls below the alarm threshold. Again, this threshold is pretty forgiving at this point, so…

Design Idea 5: Improve monitoring channel lock conditions while in TFC_HOLD state as indicated in Design Idea 4.

Design Idea 6: With fixed dither frequency and ADC pipeline delay (in terms of samples) the digital mixer output suffers a phase inversion as you vary sampling rate. The phase inversion changes the sign of the error signal, and the loop will not lock. To fix just change the sign of the return value from the Butterworth filter to maintain negative feedback. TFC seems stable thereafter, but it would be nice to know how sensitive the TFC is to this problem. Eliminating the ADC pipeline delay would be good starting point.

7. Examples: scope plots of channel locking

7.1 Basic ramp-and-lock

7.2 Power threshold issues

Design Idea 7: Instead of closing loop after backing-up to power threshold, backup to power threshold and enable zero-cross detection of phase-sensitive detector output (look for zero cross in output of Butterworth filter). Close the loop when you see the PSD zero cross. It is the peak. This scheme would permit a single, low power threshold to use only for enabling the zero-cross detector. You wouldn't need to worry about long pull-in times introduced when you close the loop at a low power level. Instead, you keep the backup ramp running until you see the zero cross, then you close the loop. Fix the ADC pipeline delay first.

8. Performance estimates

The following performance estimates are based on OPM experience and on preliminary linear loop performance demonstrated on a DSP test bed in the lab

Table 1:TFC Lock time breakdown

Item	Performance estimate	Notes
Host-to-TFC lock-to-laser command time delay	1ms	Interrupt driven, so it is fast
TFC_FIND time	2ms	Ramp filter until noise floor seen
TFC_AQUIRE	5ms	Detect valid channel power
TFC_BACKUP	10ms	Back up to the channel
TFC_PULL_IN	5ms	Linear loop pull-in
TFC_CHECK	1ms	Fill FIFO and examine sample mean
TFC_HOLD		Maintain lock
TOTAL	< 25ms	

8.1 Reset Operation

The TFC must hold the tunable optical filter steady through a SOFT reset event prompted by the host. The following table indicates how the host must operate. Holding the filter steady involves maintaining constant DAC output, meaning the TFC bus control lines must remain in a predictable, steady state throughout the RESET process.

Reset type	Conditions	Description of TFC operation
POWER ON	Circuit pack insertion (identical to HARD reset, except default state of TFC reset line is indicated.)	• Default power-on state of TFC reset line is RESET • Host init code loads TFC image into TFC RAM via HPI. • Host clears TFC state table[2] in shared memory. • Host clears TFC RESET. • TFC DSP runs from reset, recognizes cleared state table and assumes default startup state.
HARD	Host generated	• Host asserts TFC reset. • Host clears TFC state table in shared memory. • Host RESET…. • Host init code loads TFC image into TFC RAM via HPI. • Host clears TFC RESET. • TFC DSP runs from reset, recognizes cleared state table and assumes

[2] It is important that a minimum set of TFC state variables be established early, and that this set not change version-to-version, otherwise we should implement the sate table as a small, formatted database that will permit a clean reset in the event that the state information payload changes from one version to the next.

		default startup state.
SOFT[3]	Host generated (e.g., SMA agent before software download from NCP to host.)	• Host asserts TFC reset. • Host DOES NOT clear TFC state table in shared memory. • Host RESET… • Host init code loads TFC image into TFC RAM via HPI. • Host clears TFC RESET. • TFC DSP runs from reset, recognizes previous state information in state table, and assumes state(s) active just prior to reset.

[3] At host Init, register a function with the SMA agent via the

smaRebootCallbackAdd(FUNCPTR *myfunc, int arg) utility. SmaReboot() will call this function before booting new host code. The registered callback should assert the TFC reset.

9. TFC Library Details

9.1 Default constants

Approximately two-dozen parameters govern the DSP application running on the TFC. The following table groups the parameters by function. See data types in tfc_control.h. The constants defined in that file supersede values in this table, should they fall out of sync.

Table 2: TFC control loop parameters

Parameter	TFC default constant	Default Value	Units	Need mfg data	notes...
Components					
Coupler Thru	DEFAULT_COUPLER_THRU	-0.05	dB	maybe	
Coupler Drop	DEFUALT_COUPLER_DROP	-20	dB	maybe	
photodiode sensitivity	DEFAULT_PD_SENSITIVITY	0.85	Amps/W	maybe	
TIA gain	DEFAULT_TIA_GAIN	20,000	Ohms		
ADC count range	ADC_CNTS_FULL_SCALE	65,535	counts		
ADC voltage range	ADC_VOLTS_FULL_SCALE	2	volts		
ADC offset	ADC_DARK_COUNTS		counts	maybe	
Signal power threshold levels on coupler drop path					
ASE noise	DEFAULT_NOISE_POWER	-23	dBm	maybe	tweaking

Linear Loop enable power	DEFAULT_LOCK_POWER	-22	dBm	maybe	might need tweaking
Peak Lock valid power	DEFAULT_PEAK_POWER	-20			
Channel loss alarm threshold			dBm	maybe	might need tweaking
Filter Dither constants					
Dither Frequency	DEFAULT_DITHER_FREQ	3,000	Hz		
Dither pull-in Amplitude	DEFAULT_DITHER_START_AMP	200	DAC counts		
Dither hold amplitude	DEFAULT_DITHER_STOP_AMP	50	DAC counts		
Dither pull-in to hold transition time	DEFAULT_DITHER_TRANSIT_TIME	10	ms		
Open-loop channel search					
Ramp Step	DEFAULT_RAMP_STEP	200	DAC cnts per sample		
Ramp max	DEFAULT_RAMP_MAX	65,000	DAC cnts		
Ramp min	DEFAULT_RAMP_MIN	0	DAC cnts		
Samples to wait upon ramp start	DEFAULT_SAMPS2WAIT	100	samples		
Back-up start slope	DEFAULT_BACKUP_START	100	DAC cnts per sample		

Back-up end slope	DEFAULT_BACKUP_END	6	DAC cnts per sample		
Back-up slope transition	DEFAULT_BACKUP_TRANSITION	60	samples		experiment with 80. if too big will overshoot
Closed-loop parameters					
Kp (proportional gain)	DEFAULT_CLOOP_KP	0.005			
Ti (integral control parameter	DEFAULT_CLOOP_TI	0.01			
Td (derivative control parameter	DEFAULT_CLOOP_TD	0			0 means no derivative control

10. Performance Issues

10.1 Optical specifications

TFC power threshold values are arrived at using the following tables. Look for the bold values to see…

- Transmission of minimum channel power through maximum loss 1% tap
  - Pchan,min = –22 dBm
- Transmission of maximum ASE through minimum loss 1% tap.
  - Pn,max = –31.5 dBm

We need channel pull-in and lock power threshold values such that

- Pn,max < Pthresh < Pchan,min

The DEFAULT_x_POWER values in Table 2 are inside these limits. They are determined by examining the maximum and minimum scenarios in the following tables. **If your TFC is to follow and amplifier with specifications that differ from these then you must create a new table and modify the threshold parameters.**

Table 3: SDL 13dBm amplifier

	SDL 13dBm amplifier	**less filter transmission loss (3dB)**	**less 1% tap min loss of 14.5 dB**	**less 1% tap max loss of 22 dB**
Chan power	***dBm***	***dBm***	***DBm***	***dBm***
max	13	10	-4.5	-12
Min (nominal)	7	4	-10.5	-18.5
Min (extreme)	3	0	-14.5	**-22**
ASE (0.1 nm)	***dBm***			
max	-29			

ASE (250 GHz)	***dBm***			
max	-16	-19	**-33.5**	-41
Gain	***dB***			
for Pin=max	23			

Table 4: SDL 15dBm amplifier

	SDL 15dBm amplifier	less filter transmission loss	less 1% tap min loss of 14.5 dB	less 1% tap max loss of 22 dB
Chan power...	***dBm***	***dBm***	***dBm***	***dBm***
max	15	12	-2.5	-10
min (nominal)	9	5	-8.5	-16.5
min (extreme)	5	2	-12.5	-20
ASE (0.1 nm)	***dBm***			
max	-27			
ASE (250 GHz)	***dBm***			
max	-14	-17	**-31.5**	-39
Gain	***dB***			
for Pin=max	25			

Table 5: First-stage output of two stage amplifier

	first-stage output of mid-stage amp	less filter transmission loss	less 1% tap min loss of 14.5 dB	less 1% tap max loss of 22 dB
Chan power...	***dBm***	***dBm***	***dBm***	***dBm***
max	13	10	-4.5	-12
min (nominal)	7	4	-10.5	-18.5
min (extreme)	3	0	-14.5	-22
ASE (0.1 nm)	***dBm***			
max	-29			
ASE (250 GHz)	***dBm***			
max	-16	-19	-33.5	-41
Gain	***dB***			
for Pin=max	23			